



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/652,137	08/29/2003	Raymond B. Essick IV	CML00772D	1175
33117	7590	09/06/2006		EXAMINER
		LEVEQUE INTELLECTUAL PROPERTY LAW, P.C.		TRAN, DENISE
		221 EAST CHURCH ST.		
		FREDERICK, MD 21701		
			ART UNIT	PAPER NUMBER
				2185

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/652,137	ESSICK ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Denise Tran	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 19 December 2005.
- 2a) This action is **FINAL**.                                   2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-6 and 9-31 is/are rejected.
- 7) Claim(s) 7 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 29 August 2003 is/are: a) accepted or b) objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. 9/1/06.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_.

**DETAILED ACTION**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/13/06 has been entered.
2. Claims 1-31 are presented for examination.
3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claim limitations "An integrated circuit, comprising: a core processor; processing device external to the core processor; an address translation filter; and a system bus operable to link . . ." claim 9, lines 1-10 must be shown or the feature(s) canceled from the claim(s). Claims 10-13, 15-24, and 30 contain the similar problems as discussed in claim 9. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The amendment filed 6/13/06 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "An integrated circuit, comprising: a core processor; processing device external to the core processor; an address translation filter; and a system bus operable to link . . . " claim 9, lines 1-10. Claims 10-13, 15-24, and 30 contain the similar problems as discussed in claim 9.

Applicant is required to cancel the new matter in the reply to this Office Action.

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 9-13, 15-24, and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, "An integrated circuit, comprising: a core processor; processing device external to the core processor; an address translation filter; and a system bus operable to link . . ." claim 9, lines 1-10 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 10-13, 15-24, and 30 contain the similar problems as discussed in claim 9.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 9-13, 15-24, and 29-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9, line 11, it is unclear whether "the address translation unit" refers to the address translation filter or an address translation unit.

Claims 15-23, lines 2-3, it is unclear whether " the integrated circuit" refers to "integrated circuit bus" or an integrated circuit.

Claims 29-31, lines 7-11, “**an address translation filter operable to couple the processing device to the system bus**” is inconsistent to “**the address translation unit is operable to translate a virtual memory address received via the system bus from the processing device**”;

Claims 29-31 and 10-13, 24 contain the similar problems as discussed in claim 9.

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-6, 9-19, 21-22, 24-31 are rejected under 35 U.S.C. 102(a) or 102(e) as being anticipated by McDonald et al., U.S. 2003/0028751 (hereinafter McDonald).

As per claim 14, McDonald shows a digital processing system, comprising:

a core processor (e.g. fig. 1, CPU12);

an external memory unit (e.g. fig. 1, memory16);

an external processing device (e.g. fig. 3, el. 30);

an address translation filter (e.g. fig. 3, el. 32 or 40; [0054]-[0055]); and

a system bus linking the core processor, the external memory and the address translation filter to each other and linking the external processing device to the address translation filter (e.g. fig. 1, 3),

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the external processing device into a physical memory address transmitted via the system bus to the external memory unit (e.g. fig. 3, el. 32 or 40; [0054]-[0055]), wherein the bus is one of an AMBA and an AHB bus (e.g., [0029] [0083]).

As per claim 1, McDonald shows the use of an address translation filter for filtering a signal on a system bus coupled between a core processor and an external memory unit (e.g., fig. 1, system bus connected between CPU 12 and memory 16, fig. 3; el. 32, 40), the address translation filter comprising:

a first interface operable under a first bus protocol to connect to the system bus and receive a virtual memory address from an external device connected to the system bus (e.g., [0059], [0065], [0067] );

a second interface operable under a second bus protocol to connect to the system bus and transmit a physical memory address to the external memory unit (e.g. col. 5, [0054], [0049], [0029]); and

an address translation unit, external to the core processor and coupled between the first and second interfaces (e.g., fig. 3, el. 32 or 40; col. 5, [0054]), operable to determine the physical memory address from the virtual memory address (e.g., fig. 3, el. 32, 40; col. 5, [0054] [0055]),

wherein the first bus protocol is the same as the second bus protocol (e.g., [0029], [0059], [0065], [0067], [0083] ).

As per claim 15, McDonald shows a method of memory address translation in an integrated circuit bus coupled between a core processor in the integrated circuit and an external memory unit (e.g., fig. 1, [0023]), the method comprising:

receiving a first bus signal from a device in the integrated circuit via the bus in accordance with a first bus protocol (e.g., [0059], [0065], [0067], [0083]);

translating a virtual memory address specified by the first bus signal to a physical memory address in an address translation filter in the integrated circuit (e.g., fig. 3, el. 32 or 40; col. 5, [0054] [0055]; [0023]); and

transmitting a second bus signal via the bus to the external memory unit in accordance with a second bus protocol, the second bus signal specifying the physical memory address (e.g., col. 5, [0054] [0055] [0029]);

wherein the first bus protocol is the same as the second bus protocol (e.g., [0029], [0059], [0065], [0067], [0083] ).

As per claim 9, McDonald shows an integrated circuit (e.g., fig. 1, [0023]), comprising:

a core processor (e.g., fig. 1, CPU12; [0023]);  
a processing device (e.g., fig. 3, el. 30; [0023]) external to the core processor;  
an address translation filter (e.g., fig. 3, el. 32 or 40; [0023]); and  
a system bus operable to link the core processor and the address translation filter to each other under a bus protocol and to link the processing device to the address

translation filter under the same bus protocol (e.g. fig. 1, [0029], [0059], [0065], [0067], [0083]),

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the processing device into a physical memory address in an external memory unit and to transmit the physical memory address to the external memory unit via the system bus (e.g., fig. 3, el. 32 or 40; col. 5, [0054] [0055]; [0023]).

As per claim 29, McDonald shows the use of a digital processing system, comprising:

- a core processor (e.g. figure 1, CPU12)
- a processing device external to the core processor (e.g. figure 3, el. 30);
- a system bus coupled to the core processor and operable to link the core processor to an external memory unit under a system bus protocol (e.g., fig. 1, [0029]; and

- an address translation filter operable to couple the processing device to the system bus under the same system bus protocol (e.g., fig. 3, el. 32 or 40; col. 5, [0054] [0055]; [0029], [0059], [0065], [0067], [0083]);

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the external processing device into a physical memory address, in the external memory, transmitted via the system bus to the external memory unit (e.g., fig. 3, el. 32 or 40; col. 5, [0054] [0055]; [0023]).

As per claims 2-3 and 16, McDonald shows the use of the address translation

unit includes a lookup table indexed by virtual addresses and selecting a physical memory address from the table (e.g. [0054]-[0055]); the lookup table is indexed by the most significant portion of a virtual address (i.e., because the entire virtual address is used for lookup, the most significant portion is also used) (e.g. [0054]-[0055]).

As per claim 4, McDonald shows the address translation unit comprises a translation lookaside buffer (e.g. [0054]-[0055]).

As per claims 5 and 17, McDonald shows a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer (e.g. [0054]-[0055]).

As per claims 10, 25, McDonald shows wherein the address translation filter comprises: a translation lookaside buffer; and a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer (e.g. [0054]-[0055]).

As per claims 6, 11, 12-13, 18-19 and 26-28, McDonald shows the use of an output control link responsive to the refresh logic unit and operable to signal a core processor when the translation lookaside buffer is to be refreshed (e.g. [0054]-[0055]); the core processor is operable to refresh the TLB when a refresh signal is received from the address translation filter (e.g. [0054]-[0055]); the TLB is refresh via the system bus (e.g. [0054]-[0055]); refreshing comprising receiving data via the bus from the core processor coupled to the bus (e.g. [0054]-[0055]); the refreshing comprises: signaling a

core processor that the table of physical memory addresses needs to be refreshed; passing the virtual memory address to the core processor inherently; and receiving a new physical memory address from the core processor (e.g. [0054]-[0055]).

As per claims 21-22, McDonald teaches the use of the second bus signal is transmitted to the external memory unit (e.g. [0054]); the first bus signal is received from a processing device (e.g. [0054]).

Claims 24 and 30-31, McDonald shows wherein the bus is one of an AMBA bus and an AHB bus (e.g., [0029]); and the core processor, the processing device, and the address translation filter occupy the same integrated circuit (e.g., [0023]).

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over McDonald et al., U.S. 2003/0028751 (hereinafter McDonald), as applied to claims 1, 9, 14, 15, and 29 above, further in view of McGrath, U.S. Patent No. 6,671,791.

As per claim 8, McDonald does not specifically show the virtual and physical memory addresses have the same width. McGrath shows the use of the virtual and physical memory addresses have the same width. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine McGrath with

McDonald because it would provide for a reduction in the complexity of the system by removing the need to translate between the two sizes.

13. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 20 and 23 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd and paragraphs, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

15. Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (571) 272-4189. The examiner can normally be reached on Monday, Thursday, and Friday from 9:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

Art Unit: 2185

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Denise Tran

9/2/06